AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Currently amended) A semiconductor package, comprising:

a dual referenced transmission line having a predefined characteristic impedance and characteristic impedance tolerance value;

a first conductive plane;

a first dielectric layer provided between the dual referenced transmission line and the first conductive plane;

a second conductive plane;

a second dielectric layer provided between the first conductive plane and the second conductive plane, wherein an inter-plane impedance is an impedance of the first conductive plane with reference to the second conductive plane; and

wherein at least one physical parameter associated with the inter-plane impedance is selected such that the characteristic impedance value of the dual referenced transmission line does not exceed the characteristic impedance tolerance value with respect to the first and second conductive planes.

2. (Previously presented) The semiconductor package of claim 1, wherein an absolute value of a difference between a characteristic impedance of the dual referenced transmission line referenced to the first conductive plane and a characteristic impedance of the dual referenced transmission line referenced to the second conductive plane is less than the predetermined characteristic impedance tolerance value.

3. (Previously presented) The semiconductor package of claim 1, wherein the characteristic impedance of the dual referenced transmission line is calculated as a function of at least one physical parameter associated with the inter-plane impedance.

4. (Previously presented) A dual referenced transmission line having predefined characteristic impedance and characteristic impedance tolerance values, the dual referenced transmission line for transmission of a signal in a package including semiconductor circuits, wherein the dual referenced transmission line is comprised of: a signal routing trace positioned over a first reference plane, which is in turn positioned over a second reference plane, wherein an inter-plane impedance is an impedance of the first reference plane with reference to the second reference plane; and

wherein at least one physical parameter associated with the inter-plane impedance is selected such that the characteristic impedance value of the dual referenced transmission line does not exceed the characteristic impedance tolerance value with respect to the first and second reference planes.

5. (Previously presented) The dual referenced transmission line of claim 4, wherein an absolute value of a difference between a characteristic impedance of the signal routing trace referenced to the first reference plane and a characteristic impedance of the signal routing trace referenced to the second reference plane is less than the predetermined characteristic impedance tolerance value.

6. (Previously presented) The dual referenced transmission line of claim 4, wherein the characteristic impedance of the signal routing trace is calculated as a function of at least one physical parameter associated with the inter-plane impedance.

7. (Previously presented) The semiconductor package of claim 2, wherein the predetermined characteristic impedance tolerance value is two Ohms.

8. (Previously presented) The semiconductor package of claim 1, wherein the dual referenced transmission line characteristic impedance tolerance value is proportional to the inter-plane impedance.

9. (Previously presented) The semiconductor package of claim 1, wherein the dual referenced transmission line characteristic impedance tolerance value is directly proportional to

the inter-plane impedance.

10. (Previously presented) The semiconductor package of claim 1, wherein the physical parameter associated with the inter-plane impedance is at least one of: thickness of the second dielectric layer; the relative dielectric constant of the second dielectric layer; the surface area of the first and second conductive planes; the thickness of the conductive material of the first or second conductive planes; the type of conductive material of the first or second conductive planes; placement of discrete capacitors shunting the first and second conductive planes; and the number of connections which the semiconductor package makes to a die and a printed circuit board.

11. (Previously presented) The dual referenced transmission line of claim 5, wherein the predetermined characteristic impedance tolerance value is two Ohms.

12. (Previously presented) The dual referenced transmission line of claim 4, wherein the characteristic impedance tolerance value is proportional to the inter-plane impedance.

13. (Previously presented) The dual referenced transmission line of claim 4, wherein the characteristic impedance tolerance value is directly proportional to the inter-plane impedance.

14. (Previously presented) The dual referenced transmission line of claim 4, wherein the physical parameter associated with the inter-plane impedance is at least one of: thickness of a dielectric layer between the first and second reference planes; the relative dielectric constant of a dielectric layer between the first and second reference planes; the surface area of the first and second reference planes; the thickness of the conductive material of the first or second reference planes; the type of conductive material of the first or second reference planes; placement of discrete capacitors shunting the first and second reference planes; and the number of connections which a package including semiconductor circuits makes to a die and a printed circuit board having the dual referenced transmission line.